CLAIMS

What is claimed is:

1. An apparatus comprising:

a plurality of banks, each bank comprised of a plurality of memory cells organized into an array of rows and columns, wherein only one row of memory cells in each bank may be activated to be open to be accessed at any given time;

control logic coupled to the plurality of banks to control accesses made to each bank in response to commands received from an external device including a precharge command wherein banks of the plurality of banks that are affected by the precharge command are individually specified; and

a plurality of signal lines coupling the control logic to the external device able to support the precharge command using individual ones of a subset of the plurality of signal lines to individually specify the banks of the plurality of banks that are affected by the precharge command.

2. The apparatus of claim 1, wherein the subset of the plurality of signal lines used to individually specify the banks that are affected by the precharge command is comprised of row address lines also used to transmit a portion of a row address, but not used to transmit a portion of a column address as a result of the use of asymmetric addressing.

3. The apparatus of claim 2, wherein the use of the row address lines to specify the banks that are affected by the precharge command is enabled through programming a register within the control logic.

4. The apparatus of claim 3, wherein the plurality of signal lines used to individually specify the banks that are affected by the precharge command is further comprised of bank address lines otherwise used to transmit a portion of a bank address in support of an alternate precharge command, and wherein the programming of a register within the control logic to enable the use the row address lines to individually specify the banks that are affected by the precharge command also results in disabling the use of the bank address lines to support the alternate precharge command and in enabling the use of the bank address lines to individually specify the banks that are affected by the precharge command.

5. The apparatus of claim 2, wherein the precharge command is received by the control logic as part of an autoprecharge command embedded within an access command received by the control logic.

6. A computer system comprising:

a CPU;

a memory device having a plurality of banks, each bank comprised of a plurality of memory cells organized into an array of rows and columns, wherein the memory device is capable of closing open rows in banks individually specified in a precharge command;

a memory bus comprised of a plurality of signal lines coupled to the memory device; and

a memory controller coupled to the CPU and to the memory bus to transmit the precharge command to the memory device across the memory bus wherein banks within the memory device having an open row to be closed in response to the precharge command are individually specified through corresponding individual ones of a subset of the plurality of signal lines of the memory bus.

7. The computer system of claim 6, in which each of the subset of signal lines used in the precharge command to individually specify a bank in which an open row is to be closed is comprised of row address lines also used to transmit a portion of a row address, but not a portion of a column address, as a result of asymmetric addressing.

8. The apparatus of claim 7, wherein the memory controller is further comprised of a control register programmable by the CPU to enable the use of the row address lines to individually specify banks having an open row to be closed in the precharge command.

9. A method comprising:

determining whether or not there is a bank within a plurality of banks within a memory device having an open row that must be closed in preparation for an upcoming access command; and

transmitting a precharge command to the memory device through a subset of signal lines of a memory bus comprised of a plurality of signal lines using individual ones of the subset of signal lines to individually specify at least one bank within the memory device having an open row that is to be closed.

10. The method of claim 9, wherein determining whether or not there is a bank within a memory device having an open row that must be closed in preparation for an upcoming access command further comprises parsing a queue of upcoming access commands to determine which row must be open in each bank within the plurality of banks within the memory device in preparation for a given upcoming access command within the queue.

11. The method of claim 9, wherein determining whether or not there is a bank within a memory device having an open row that must be closed in preparation for an upcoming access command further comprises employing at least one prediction algorithm to predict which row must be open in each bank within the plurality of banks within the memory device in preparation for an upcoming predicted access command.

12. The method of claim 9, further comprising configuring a memory controller to use a plurality of signal lines to individually specify at least one bank within the memory device in which an open row must be closed, as an alternative to using a plurality of bank address lines to transmit a binary code specifying no more than one bank within a memory device in which an open row must be closed.

13. The method of claim 9, wherein transmitting the precharge command to the memory device further comprises embedding the precharge command in an access command as an autoprecharge command to cause the precharge command to be carried out immediately after the access command is carried out.

14. A machine-accessible medium comprising code that when executed by a processor within an electronic device, causes the electronic device to:

carry out a test of a memory device to determine whether or not the memory device supports a precharge command in which individual ones of a subset of signal lines of a memory bus comprised of a plurality of signal lines are used to individually specify at least one of a plurality of banks comprising the memory device having an open row of memory cells that is to be closed; and

program a memory controller coupling the memory device to the CPU to enable the use of a precharge command in which individual ones of the subset of signal lines are used to individually specify at least one of the plurality of banks as an alternative to using a plurality of bank address lines to transmit a binary code across the memory bus specifying only one bank of the plurality of banks having an open row of memory cells that is to be closed in an alternate form of precharge command.

15. The machine-accessible medium of claim 14, further causing the processor to program the memory controller to enable the use of the bank address lines to comprise at least a portion of the subset of signal lines, and to disable the use of the bank address lines to transmit the binary code specifying only one bank of the plurality of banks.